CLAIMS

We claim:

1. A method for processing electrical signals, comprising:

applying an input signal to a source follower;

sensing drain current of the source follower;

multiplying the sensed drain current; and

applying the multiplied sensed drain current to an output of the source follower.

2. The invention of claim 1, wherein a folded cascode device senses the drain current.

3. The invention of claim 1, wherein a current mirror multiplies the sensed drain current.

4. The invention of claim 3, wherein the source follower and the current mirror are both implemented using a single type of device.

5. The invention of claim 4, wherein the source follower and the current mirror are both implemented using NMOS devices.

6. A circuit comprising:

a source follower;

a first device connected to sense drain current of the source follower; and

a current mirror connected to multiply the sensed drain current for application to an output of the source follower.

7. The invention of claim 6, wherein the first device is a folded cascode device.

8. The invention of claim 6, wherein the source follower and the current mirror are both implemented using a single type of device.

9. The invention of claim 8, wherein the source follower and the current mirror are both implemented using NMOS devices.

10. The invention of claim 6, wherein the circuit is an integrated circuit.

11. A circuit comprising:

a transistor M3;

a transistor M2 connected at a first channel node to a second channel node of the transistor M3, wherein:

a gate node of the transistor M2 is connected to an input VIN; and

a second channel node of the transistor M2 is connected to an output VOUT;

a transistor M0 connected at a first channel node to the output VOUT;

a transistor M4 connected at a first channel node to the second channel node of the transistor M3; and

a transistor M1 connected at a first channel node and a gate node to a second channel node of the transistor M4 and to a gate node of the transistor M0, wherein a second channel node of the transistor M1 is connected to a second channel node of the transistor M0.

12. The invention of claim 11, wherein, when (1) a first channel node of the transistor M3 is connected to a first supply voltage, (2) the second channel nodes of the transistors M0 and M1 are connected to a second supply voltage, (3) a gate node of the transistor M3 is connected to a first gate bias voltage, and (4) a gate node of the transistor M4 is connected to a second gate bias voltage, an output voltage appearing at the output VOUT is proportional to an input voltage applied at the input VIN.

13. The invention of claim 12, wherein the first supply voltage is Vdd, and the second supply voltage is ground.

14. The invention of claim 12, wherein:

the transistor M3 functions as a current source for the circuit;

the transistors M0 and M2 function as a source follower;

the transistors M0 and M1 function as a current mirror;

the transistor M4 senses a drain current at the transistor M2; and

the current mirror multiplies the sensed drain current and applies the multiplied sensed drain current to the output VOUT.

15. The invention of claim 11, wherein:

the transistors M0, M1, and M2 are of a first type; and

the transistors M3 and M4 are of a second type different from the first type.

16. The invention of claim 15, wherein the first type is NMOS transistors and the second type is PMOS transistors.

17. The invention of claim 14, wherein the source follower and the current mirror are both implemented using a single type of device.

18. The invention of claim 17, wherein the source follower and the current mirror are both implemented using NMOS devices.

19. The invention of claim 11, wherein the circuit is an integrated circuit.